10-26-00

A

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Title of Invention	**MARKING METHOD FOR SEMICONDUCTOR WAFER**
Named Inventor(s)	**SATOSHI KITAGAWA**
Attorney Docket	**45484 - 247805**
Express Mail Label No.	**EL561434843US**

APPLICATION ELEMENTS

1. ☒ Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. ☒ Specification, Claims, and Abstract — Total Pages **23**
3. ☒ Drawings — Total Sheets **6**
4. Oath or Declaration — Total Pages
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* **[Note Box 5 Below]**
      (i) ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation by Reference *(usable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement *(when there is an assignee)*
   ☐ Power of Attorney by assignee
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement (IDS) PTO-1449
    ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. ☐ Small Entity Statement(s)
    ☐ Statement filed in prior application Status still proper and desired
15. ☒ Certified Copy of Priority Document(s)
16. ☐ Other:

17. If a **CONTINUING APPLICATION**, *check appropriate box and supply the requisite information:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:

18. CORRESPONDENCE ADDRESS:

Roger T. Frost
KILPATRICK STOCKTON LLP
3424 Peachtree Road, N.E.
2400 Monarch Tower
Atlanta, GA 30326
Telephone: 404-949-2400
Facsimile: 404-949-2499

By: _____ Reg. No. 22,176
Date: October 25, 2000

FEE TRANSMITTAL

Attorney Docket No. **45484 - 247805**

This sheet accompanies a patent application transmittal for the following application:

Inventor: **SATOSHI KITAGAWA**
Filing Date: **October 25, 2000**
Title: **Marking Method for Semiconductor Wafer**

The filing fee is calculated as shown below:

1. **FILING FEE:**

	SMALL ENTITY		LARGE ENTITY	
FOR:	FEE	FEE PAID	FEE	FEE PAID
☐ UTILITY FILING FEE			**710**	**710**
☐ DESIGN FILING FEE				
☐ PLANT FILING FEE				
☐ REISSUE FILING FEE				
☐ PROVISIONAL FILING FEE				
SUBTOTAL (1)				**$710.00**

2. **CLAIMS:**

			SMALL ENTITY		LARGE ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE	RATE	FEE
TOTAL CLAIMS	25 - 20 =	5			18.00	**90.00**
INDEP. CLAIMS	5 - 3 =	2			80.00	**160.00**
☐ MULTIPLE DEPENDENT CLAIM PRESENTED						
SUBTOTAL (2)						**$250.00**

3. **ADDITIONAL FEES:**

	SMALL ENTITY		LARGE ENTITY	
FOR:	FEE	FEE PAID	FEE	FEE PAID
☐ LATE FILING, FEE OR OATH				
☐ NON-ENGLISH SPECIFICATION				
☐ OTHER				
SUBTOTAL (3)				

TOTAL FILING FEES: $ 960.00

A check is enclosed for the total amount: **$ 960.00**

☐ Charge any additional fees required under 37 C.F.R. 1.16 or 1.17 to Deposit Account 10-1215.

KILPATRICK STOCKTON, LLP
3424 Peachtree Road, N.E.
Atlanta, Georgia 30326
Telephone: 404-949-3339

By: _____ Date: **October 25, 2000**

Roger T. Frost, Attorney for Applicant
Reg. No. 22,176

MARKING METHOD FOR SEMICONDUCTOR WAFER

Background of the Invention

Field of the Invention

The present invention relates to a method for appropriately marking a semiconductor wafer in order to enable correct identification of the semiconductor wafer, as well as to a semiconductor wafer marked by said method.

Background Art

In the event failures are found to have arisen during the course of manufacture or after shipment of semiconductor wafers, such as silicon wafers, accurate reporting of the failures to a manufacturing facility is very important for determining sources of the failures without fail.

In order to enable such feedback, individual wafers which are under manufacture must be identifiable. To this end, individual semiconductor wafers are marked at initial stages in the process of manufacture.

Marking of semiconductor wafers is usually implemented, by means of making a certain impression on specified locations of individual wafers which are under manufacture. In order to achieve this, a laser marking machine (described in, for example, Japanese Patent Application Laid-Open Nos. 23512/1984 and 175154/1990), for example, is used.

A typical mark to be inscribed on an individual wafer is an ID number. There may be a case where a mark, such as a bar code, a character, or a numeral, is inscribed on the surface

of a wafer as information about processing conditions, processing history, or electrical properties. In this case, a mark can be used for process and production control, as well as for tracing the source and route of failures. Consequently, wafers can be identified during the course of manufacture or after shipment.

A marking operation involves application of any physical action to a wafer which is under manufacture. For this reason, there may arise a case where slips arise in a wafer for reasons of marking operation. In order to prevent an adverse effect on a wafer, which would otherwise be imposed by a marking operation, marking a wafer on the smallest possible scale is preferable.

Inscription of a minute mark is preferable in terms of protection of a wafer from an adverse effect. However, a minute mark is easily effaced by surface treatment to which a semiconductor wafer is to be subjected during the course of manufacturing process. Needless to say, manufacture of semiconductor wafers is incessantly performed on a production line. If a semiconductor wafer whose mark is effaced is mingled with other semiconductor wafers, finding the semiconductor wafer and restoring the thus-found wafer to its original condition is very difficult.

The present invention has been conceived in light of the foregoing problems and is aimed at providing a method of inscribing marks on a semiconductor wafer, which marks are less susceptible to surface treatment performed during the course of manufacture, as well as a semiconductor wafer for distribution.

Summary of the Invention

To solve the above-described drawbacks, the present invention provides a marking method for inscribing a plurality of minute ID marks on a wafer which function as mutual backups.

Preferably, identical marks are formed in two or more locations on a semiconductor wafer for distribution purpose. These marks act as backup marks such that, if one of the marks is effaced, the remaining mark(s) acts as a backup. Even in a case where one of the marks is effaced by means of surface treatment to which the semiconductor wafer is to be subjected to during the course of manufacture, the original mark can be immediately and correctly restored.

More specifically, the present invention is to provide the followings:

(1) A method of reproducing a mark on a semiconductor wafer, wherein, in a case where a predetermined mark which has been made on a semiconductor wafer beforehand during the course of manufacture or processing is substantially effaced in association with progress of manufacturing operation or processing operation, a mark essentially identical with the substantially-effaced mark is formed at another location spaced apart from the substantially-effaced mark.

(2) A method of reproducing a mark on a semiconductor wafer, wherein, in a case where any one of predetermined single essentially-identical marks which have been made in two or more locations on a semiconductor wafer beforehand during the course of manufacture or processing is substantially effaced in

association with progress of manufacturing operation or processing operation, a mark essentially identical with the substantially-effaced mark is reproduced by reference to the substantially-remaining other mark.

(3) The method of reproducing a mark on a semiconductor wafer according to (2), wherein the substantially-effaced mark is reproduced by means of forming a mark essentially identical with the substantially-effaced mark at another location spaced apart from the substantially-effaced mark.

(4) The method of reproducing a mark on a semiconductor wafer according to (1) or (3), wherein the another location corresponds to a location in the vicinity of the substantially-effaced mark.

(5) The method of reproducing a mark on a semiconductor wafer according to (4), wherein the predetermined mark is formed by means of a combination of dots, each dot measuring 1 to 13 μm.

(6) The method of reproducing a mark on a semiconductor wafer according to (5), wherein the predetermined mark is a minute ID mark.

(7) The method of reproducing a mark on a semiconductor wafer according to (6), wherein the predetermined mark is a mark affixed on the interior wall surface of a notch.

(8) A semiconductor wafer for distribution purpose having two or more essentially-identical marks formed thereon.

(9) The semiconductor wafer for distribution purpose according to (8), wherein two or more essentially-identical marks

are provided at positions where the marks are to undergo the same surface treatment at different speeds during the course of manufacture.

(10) The semiconductor wafer for distribution purpose according to (9), wherein two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other identical marks are provided on the reverse side of the same.

(11) The semiconductor wafer for distribution purpose according to (10), wherein two or more essentially-identical marks are provided close to each other.

(12) The semiconductor wafer for distribution purpose according to any one of (8) through (10), wherein two or more essentially-identical marks are provided within an area where a single optical reading machine can read the marks simultaneously.

(13) The semiconductor wafer for distribution purpose according to anyone of (8) through(12), wherein two or more essentially-identical marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm.

(14) The semiconductor wafer for distribution purpose according to (13), wherein the marks are ID marks.

(15) The semiconductor wafer for distribution purpose according to (13) or (14), wherein the predetermined marks are affixed on the interior wall surface of a notch.

(16) The semiconductor wafer for distribution purpose according to (13), wherein the marks are for positioning purpose.

(17) The semiconductor wafer for distribution purpose according to (13), wherein the marks are provided for suggesting crystal orientation of the semiconductor wafer.

(18) The semiconductor wafer for distribution purpose according to (16) or (17), wherein the semiconductor wafer is perfectly annular.

(19) A wafer carrier storing the semiconductor wafers for distribution purpose defined in (12) while the marks are aligned with each other.

(20) Use of a semiconductor wafer on which two or more essentially-identical marks are formed by means of marking the semiconductor wafer during the course of manufacture or processing.

(21) A method of obviating a demerit, which would otherwise be caused when a single mark is substantially effaced in association with manufacture or processing of a semiconductor wafer, by means of marking a semiconductor wafer with two or more essentially-identical marks during the course of manufacture or processing.

In connection with the concept regarding "processes for manufacturing or processing a semiconductor wafer," the expression "process for manufacturing a semiconductor wafer" used herein encompasses all processes pertaining to manufacture of a semiconductor wafer. Further, the expression "process for processing a semiconductor wafer" encompasses all processes pertaining to processing of a semiconductor wafer manufactured by way of the semiconductor wafer manufacturing process, such

as a process of processing into a semiconductor device a semiconductor wafer manufactured by way of the semiconductor wafer manufacturing process.

The expression "substantially effaced" and the expression "substantial effacement" encompass a case where a mark is not effaced completely but is difficult to detect or read, as well as a case where a mark is completely effaced. Further, the expression "effacement" used herein often means a case where a mark is not effaced completely but is difficult to detect or read, as well as a case where a mark is completely effaced.

The expression "substantially identical mark" is a concept encompassing not only a completely identical mark, but also a mark which is identical with respect to a portion required for identifying a semiconductor wafer but which differs in other respects, such as an additional portion. For instance, such a mark corresponds to a mark which is identical with respect to portions expressing a lot number and a serial number assigned to a semiconductor wafer but which differs with respect to only a portion expressing the number of times the mark is reproduced.

The present embodiment includes a case where a substantially-remaining mark is fully copied to another location, as well as a case where a portion required for identifying a semiconductor wafer is extracted from a substantially-remaining mark, an additional portion is changed, as required, and the mark is inscribed at another location along with the thus-changed additional portion.

The expression "predetermined mark" typically designates

an ID number assigned to an individual wafer. Further, the expression covers a mark expressing the processing history of a wafer, such as a bar code, a character, or a numeral. Further, the expression "predetermined mark" may correspond to a registered trademark.

The expression "substantially effaced" means a case where a mark is effaced to such an extent that the mark is difficult to detect or read, as well as a case where a mark is completely effaced.

The present invention is aimed at processing a wafer. Here, processing of a wafer can be carried out without regard to the constituent components of a wafer. The object of the present invention is not limited to a silicon wafer; the present invention can be applied to wafers of all types and forms; for example, wafers made of different raw materials such as compound semiconductor wafers; wafers produced by way of different processes such as nitrogen-doped wafers; and wafers which have been subjected to special treatment such as epitaxial wafers which are sliced after having been epitaxially grown.

The expression "semiconductor wafer for distribution purpose" means a semiconductor wafer which is used not only for test or research purposes but also for commercial circulation.

The expression "front and reverse" signifies respective surfaces of a wafer having an edge therebetween. The expression "front side" means a front surface as well as a front bevel surface, and the expression "reverse side" means a reverse surface as well as a reverse bevel surface.

The expression "perfect annular wafer" means a wafer devoid of a notch or an orientation flat.

Brief Description of the Drawings

FIG. 1 shows the functional construction of a common laser marking machine;

FIG. 2 shows the functional construction of a common reading machine;

FIG. 3 is an example of a mark;

FIGS. 4A and 4B are illustrations for describing marking locations;

FIG. 5 is an enlarged cross-sectional view for describing marking positions; and

FIGS. 6A and 6B are illustrations for describing storage of wafers in a wafer carrier.

Detailed Description of the Preferred Embodiment

A preferred embodiment of the present invention will be described hereinbelow by reference to the accompanying drawings.

[Marking Machine]

All marking machines which are currently available can be used for implementing a marking method according to the present invention. In the present embodiment, a laser marking machine is taken as a typical example.

As shown in FIG. 1, a laser marking machine is usually equipped with an optical element 11 consisting of a laser-beam inlet optical system and a lens for defining a mask geometry;

a liquid-crystal mask 13; and a projection lens 14 which guides a laser beam to a wafer W and forms the image of the liquid-crystal mask 13 at a predetermined location on the wafer W.

In such a laser marking machine, the position of projection of the projection lens 14 is adjusted, to thereby produce an image corresponding to a desired mark on the liquid-crystal mask 13. The liquid-crystal mask 13 is exposed to a laser beam, wherewith a desired mark can be made on the wafer W.

A laser marking machine described in Japanese Patent Application Laid-Open No. 19737/1999 is particularly preferable, because it can make a ultra-minute mark.

[Reading Machine]

A mark made on the wafer W by means of such a laser marking machine is read by a reading machine.

As shown in FIG. 2, a popular reading machine radiates a laser beam originating from a light source 21 onto a mark inscribed on the wafer W, and light reflected by the mark is focused to produce an image by way of an imaging lens 23. The thus-formed image is detected by a camera 24, as a result of which the mark on the wafer W is read.

The mark on the wafer W corresponds to, for example, a mark such as that shown in FIG. 3. The reading machine shown in FIG. 2 reads the mark.

[Marking Position]

As shown in FIG. 4, in the present embodiment, marks are affixed on two locations on the interior wall surface of a notch 31 of the wafer W (A1 and A2 shown in FIG. 4A or B1 and B2 shown

in FIG. 4B).

FIG. 5 is an enlarged cross-sectional view of the wafer W. As illustrated, there are five candidate making locations; a front surface 31a; a front bevel surface 31b; an edge 31c; a reverse bevel surface 31d; and a reverse surface 31e. Two marks A1 and A2 shown in FIG. 4A differ in location from each other with reference to the circumferential direction of the notch 31. Further, mark A1 is formed on a front bevel surface, and mark A2 is formed on an edge. Thus, marks A1 and A2 differ in level with reference to the vertical direction.

Similarly, of two marks B1 and B2 shown in FIG. 4B, mark B1 is formed on a front bevel surface, and mark B2 is formed on a reverse bevel surface.

As will be stated in connection with an example which will be described later, in a case where a wafer is to be subjected to surface treatment during the course of manufacture, a difference exists between a mark printed on the front surface of a wafer and a mark printed on a front bevel surface of a wafer, as well as between a mark printed on the front surface of a wafer and a mark printed on the reverse surface of a wafer, in terms of an extent to which a mark is effaced. It is also admitted that effacement of a mark changes according to types of manufacturing processes to which a wafer is to be subjected.

According to the present invention, two or more marks are made on a wafer which act as mutual backup. If one of the two or more marks is completely effaced or effaced to such an extent that a reading machine cannot read the mark, another mark identical

with the remaining mark is newly inscribed on a wafer, thus restoring the wafer to its original condition.

Thus, the present invention prevents occurrence of a problem, such as loss of a wafer or the impossibility of tracing a wafer, which would otherwise be caused when a mark is effaced during the course of manufacture, by means of constantly ensuring two or more marks on a wafer.

[Marked Wafer]

The above embodiment describes an example in which two marks are made on a wafer. However, three or more marks may also be formed.

So long as a plurality of marks are formed within a narrow area where a single reading machine can read these marks simultaneously, detection efficiency is improved. Concentration of marks in a narrow area is also preferable in terms of improvement in processing efficiency. In a case where a plurality of wafers W are stored in a wafer carrier 41 for transportation, aligning positions of marks on wafers W is preferable, for the same reasons (FIGS. 6A and 6B).

In a case where a mark identical with an original mark which has been effaced is newly made on a wafer in order to restore the original mark, if the original mark remains incompletely effaced, making a new mark on another location spaced apart from the location of the original mark is preferable, in order to prevent occurrence of interference which would otherwise arise between the original mark and the new mark. At that time, if the new mark is formed in a position spaced apart from the original

mark and in the vicinity thereof, the new mark can stay within the view field of the reading machine.

[Example]

Identical marks having a width of 320 μm were formed on the front and front bevel surfaces of a wafer W, the front and reverse bevel surfaces of an interior of a notch, and the reverse bevel surface of the interior of the notch. After formation of a thin copper film of 1 μm thickness on the wafer W, the wafer W was subjected to CMP (chemical-and-mechanical polishing). The extent to which marks were effaced (i.e., the extent to which marks remain) was observed twice; i.e., after formation of the thin copper film and after CMP.

Observation results are provided in Table 1.

TABLE 1

	AFTER FORMATION OF THIN COPPER FILM OF 1 μm THICKNESS	AFTER CMP BY 0.75 μm
FRONT SURFACE	CLEARLY READABLE	COMPLETELY EFFACED
FRONT BEVEL SURFACE	DIFFICULT TO READ	DIFFICULTY TO READ
FRONT BEVEL SURFACE OF INTERIOR OF NOTCH	CLEARLY READABLE	SLIGHTLY DIFFICULT TO READ
REVERSE BEVEL SURFACE	CLEARLY READABLE	CLEARLY READABLE
REVERSE BEVEL SURFACE OF INTERIOR NOTCH	CLEARLY READABLE	CLEARLY READABLE

As can be seen from the observation results provided in Table 1, after the wafer W has been subjected to CMP, both the mark on the front bevel surface of the notch and the mark on the reverse bevel surface of interior of the notch remain readable

well, regardless of whether the marks are present on the exterior or interior of the notch. In a case where the mark on the reverse side of the notch has been effaced by debris on the reverse side, the mark on the front surface acts as a backup mark.

So long as a mark on the front bevel surface and the mark on the reverse bevel surface are sufficiently close to each other with reference to the circumferential direction of the notch, regardless of whether the marks are present on the interior or exterior of the notch, the marks can sufficiently fall within a single view field of a camera. Thus, even when a plurality of marks are located within an area where they back each other up, a single camera can observe the marks simultaneously.

In a semiconductor wafer according to the present invention, a plurality of marks are formed for mutual backup. Therefore, even in a case where ultra-minute marks are made on a semiconductor wafer, there can be prevented confusion due to effacement of a mark and there can be eliminated worry about the impossibility of tracing a semiconductor wafer.

CLAIMS

1. A method of reproducing a mark on a semiconductor wafer, wherein, in a case where a predetermined mark which has been made on a semiconductor wafer beforehand during the course of manufacture or processing is substantially effaced in association with progress of manufacturing operation or processing operation, a mark essentially identical with the substantially-effaced mark is formed at another location spaced apart from the substantially-effaced mark.

2. A method of reproducing a mark on a semiconductor wafer, wherein, in a case where any one of predetermined single essentially-identical marks which have been made in two or more locations on a semiconductor wafer beforehand during the course of manufacture or processing is substantially effaced in association with progress of manufacturing operation or processing operation, a mark essentially identical with the substantially-effaced mark is reproduced by reference to the substantially-remaining other mark.

3. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the substantially-effaced mark is reproduced by means of forming a mark essentially identical with the substantially-effaced mark at another location spaced apart from the substantially-effaced mark.

4. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the substantially-effaced mark is reproduced by means of forming a mark essentially identical

with the substantially-effaced mark at another location in the vicinity of the substantially-effaced mark.

5. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is formed by means of a combination of dots, each dot measuring 1 to 13 μm, and the substantially-effaced mark is reproduced by means of forming a mark essentially identical with the substantially-effaced mark at another location in the vicinity of the substantially-effaced mark.

6. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is a minute ID mark which is assigned to the semiconductor wafer and is formed by means of a combination of dots, each dot measuring 1 to 13 μm, and the substantially-effaced mark is reproduced by means of forming a mark essentially identical with the substantially-effaced mark at another location in the vicinity of the substantially-effaced mark.

7. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is a mark affixed on the interior wall surface of a notch.

8. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is a mark affixed on the interior wall surface of a notch, and the substantially-effaced mark is reproduced by means of forming a mark essentially identical with the substantially-effaced mark at another location spaced apart from the substantially-effaced mark.

9. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is a mark affixed on the interior wall surface of a notch, and the substantially-effaced mark is reproduced by means of forming a mark essentially identical with the substantially-effaced mark at another location in the vicinity of the substantially-effaced mark.

10. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is formed by means of a combination of dots, each dot measuring 1 to 13 μm and is affixed on the interior wall surface of a notch, and the substantially-effaced mark is reproduced by means of forming a mark essentially identical with the substantially-effaced mark at another location in the vicinity of the substantially-effaced mark.

11. The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is an ID mark which is assigned to the semiconductor wafer, is formed by means of a combination of dots, each dot measuring 1 to 13 μm, and is affixed on the interior wall surface of a notch, and the substantially-effaced mark is reproduced by means of forming a mark essentially identical with the substantially-effaced mark at another location in the vicinity of the substantially-effaced mark.

12. A semiconductor wafer for distribution purpose having two or more essentially-identical marks formed thereon.

13. The semiconductor wafer for distribution purpose

according to claim 12, wherein two or more essentially-identical marks are provided at positions where the marks are to undergo the same surface treatment at different speeds during the course of manufacture.

14. The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture.

15. The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks are located close to each other and such that the marks undergo the same surface treatment at different speeds during the course of manufacture.

16. The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read

the marks simultaneously.

17. The semiconductor wafer for distribution purpose according to claim 12, wherein two or more essentially-identical marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm, and some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

18. The semiconductor wafer for distribution purpose according to claim 12, wherein two or more essentially-identical marks are minute ID marks which are assigned to the semiconductor wafer and are formed by means of a combination of dots, each dot measuring 1 to 13 μm, and some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

19. The semiconductor wafer for distribution purpose according to claim 12, wherein two or more essentially-identical marks are minute ID marks which are assigned to the semiconductor

wafer, are formed by means of a combination of dots, each dot measuring 1 to 13 μm, and are affixed on the interior wall surface of a notch, and some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

20. The semiconductor wafer for distribution purpose according to claim 12, wherein two or more essentially-identical marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm for positioning purpose, and some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

21. The semiconductor wafer for distribution purpose according to claim 12, wherein two or more essentially-identical marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm and indicate crystal orientation of the semiconductor wafer, and some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks

are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

22. The semiconductor wafer for distribution purpose according to claim 12, wherein the semiconductor wafer is perfectly annular; two or more essentially-identical marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm and indicate crystal orientation of the semiconductor wafer; and some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

23. The semiconductor wafer for distribution purpose according to claim 12, wherein two or more essentially-identical marks are aligned in a single direction; and some of two or more essentially-identical marks are provided on the front side of the semiconductor wafer and the other essentially-identical marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

24. Use of a semiconductor wafer on which two or more essentially-identical marks are formed by means of marking the semiconductor wafer during the course of manufacture or processing.

25. A method of obviating a demerit, which would otherwise be caused when a single mark is substantially effaced in association with manufacture or processing of a semiconductor wafer, by means of marking a semiconductor wafer with two or more essentially-identical marks during the course of manufacture or processing.

ABSTRACT OF THE DISCLOSURE

A plurality of minute ID marks are inscribed on a semiconductor wafer which is under manufacture, without imposing adverse effect to the wafer, in order to make the marks less susceptible to surface treatment to be performed during the course of manufacture. Further, the minute ID marks act as mutual backups. Inscribing such minute ID marks on a semiconductor wafer prevents confusion due to effacement of ultra-minute marks and eliminates worry about the impossibility of tracing a semiconductor wafer.

Attorney docket No.: 45484 / 247805

FIG.1

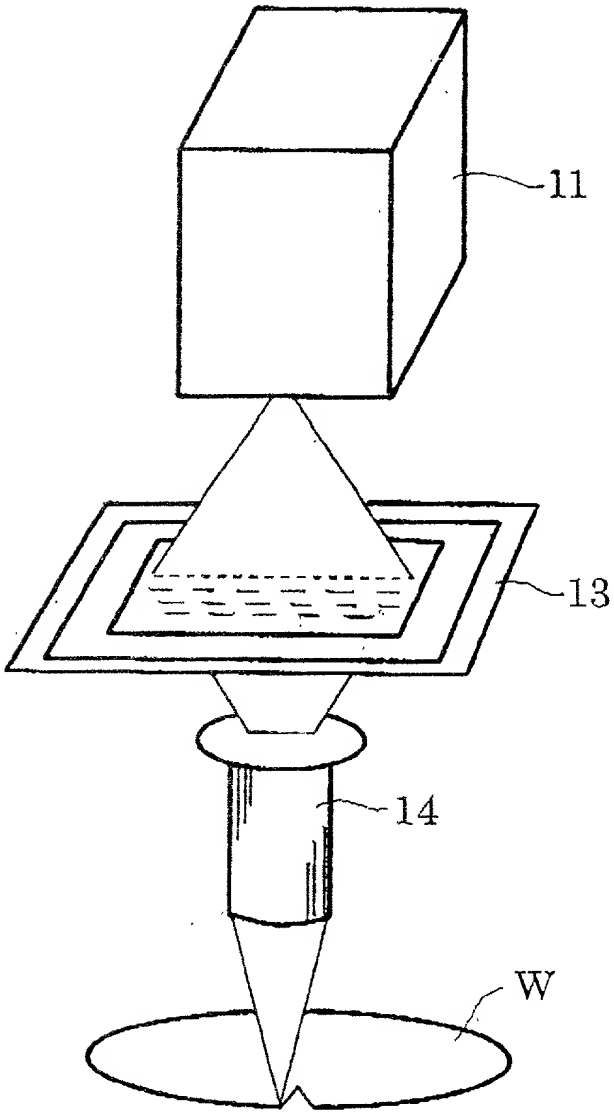


FIG.2

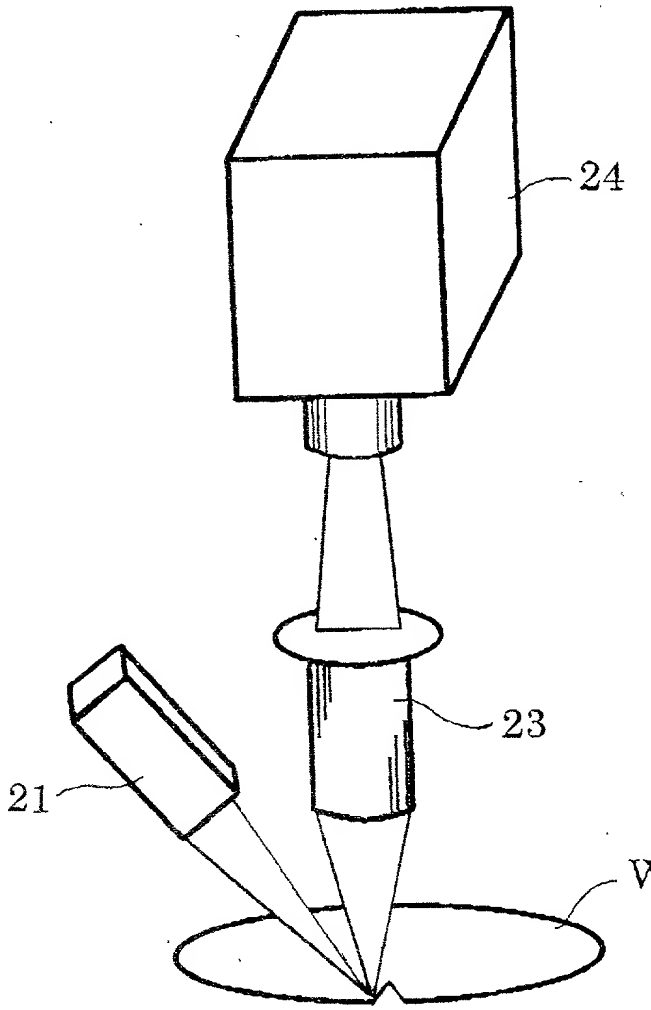


FIG.3

FIG.4

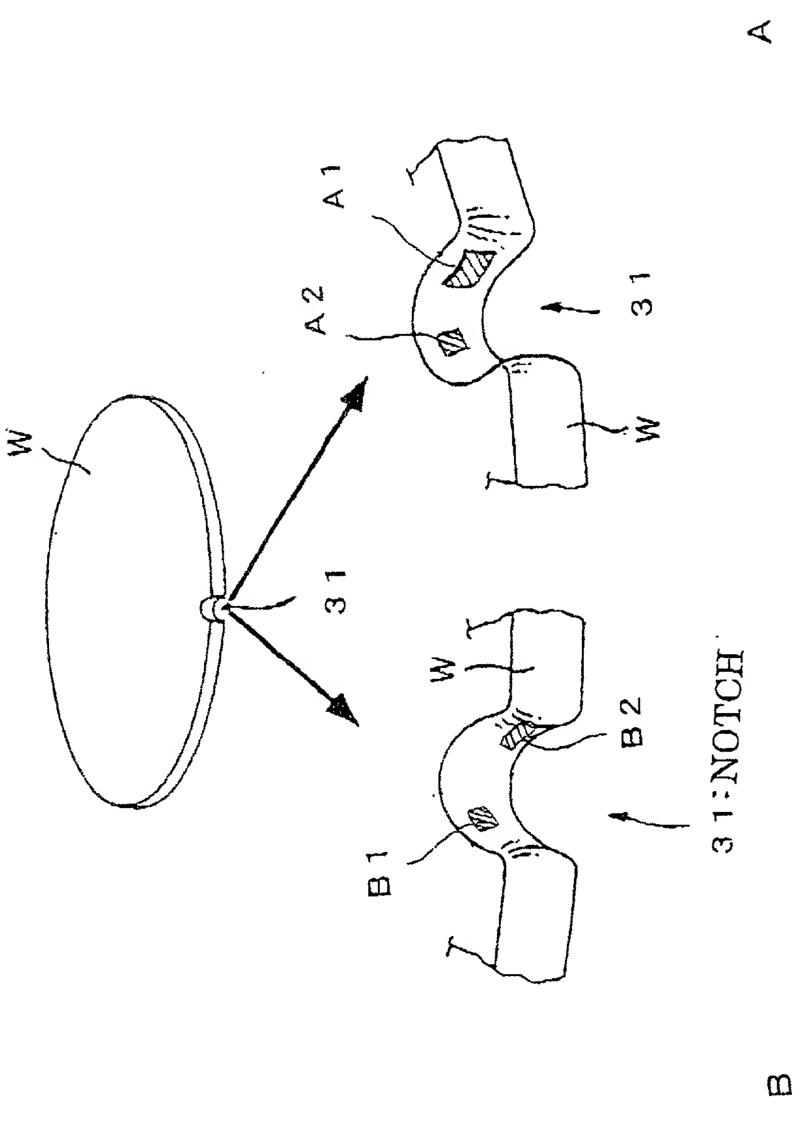


FIG.5

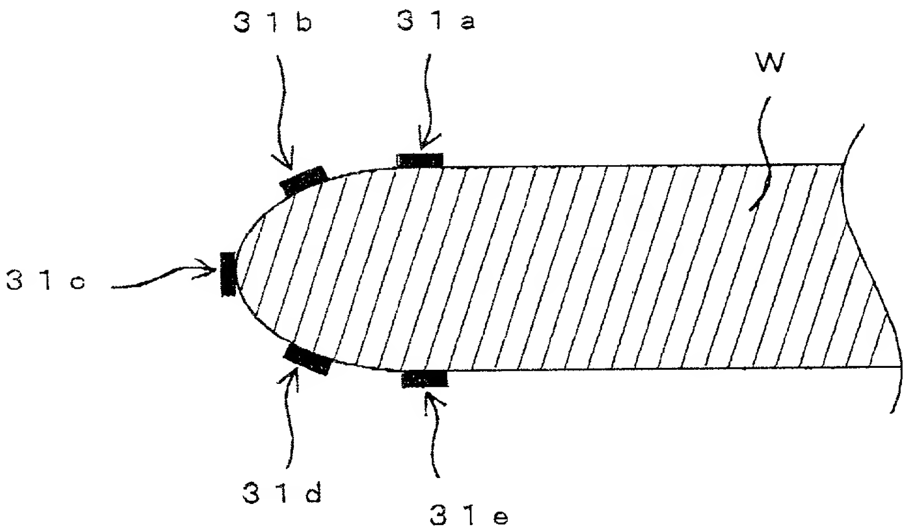


FIG.6 A

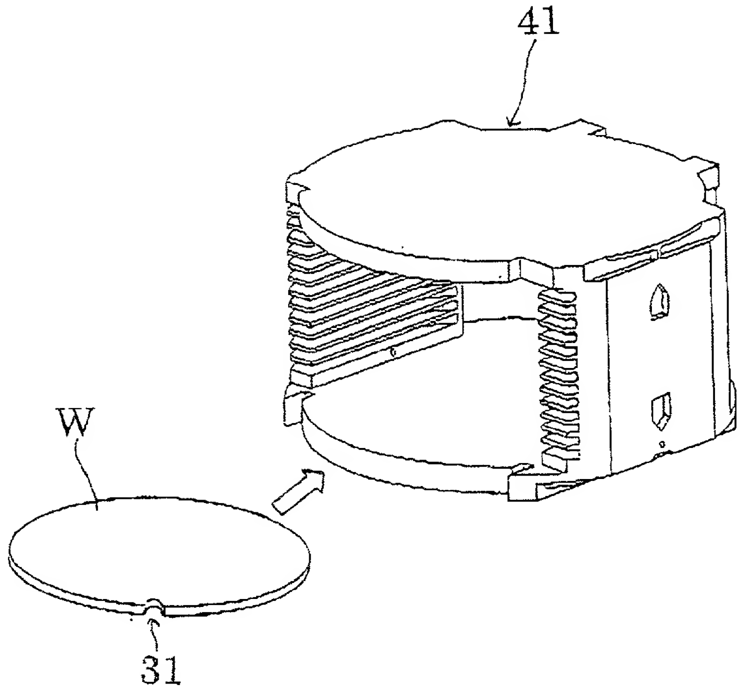
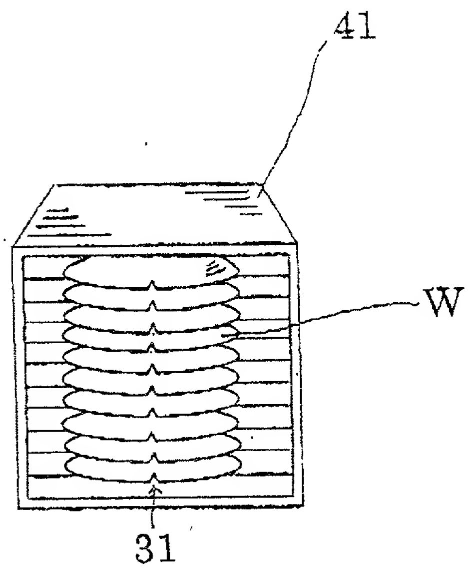


FIG.6 B



Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状

Japanese Language Declaration
日本語宣言書

私は、以下に記名された発明者として、ここに以下の通り宣言する。

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先そして国籍は、私の氏名の後に記載された通りである。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明について、特許請求範囲に記載され、且つ特許が求められている発明主題に関して、私は、最初、最先且つ唯一の発明者である（唯一の氏名が記載されている場合）が、或いは最初、最先且つ共同発明者である（複数の氏名が記載されている場合）と信じている。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

MARKING METHOD FOR SEMICONDUCTOR WAFER

上記発明の明細書はここに添付されているが、下記の欄がチェックされている場合はこの限りでない：

the specification of which is attached hereto unless the following box is checked:

☐ _____の日に出願され、この出願の米国出願番号またPCT国際出願番号は、_____であり、且つ_____の日に補正された出願（該当する場合）

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

私は、上記の補正書によって補正された、特許請求範囲を含む上記明細書を検討し、且つ内容を理解していることをここに表明する。

I hereby states that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編規則1.56に定義されている、特許性について重要な情報を開示する義務があることを認める。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese language Declaration
(日本語宣言書)

私は、ここに、以下に記載した外国での特許出願または発明者証の出願、或いは米国以外の少なくとも一国を指定している米国法典第35編第365条(a)によるPCT国際出願について、同第119条(a)-(d)項又は第365条(b)項に基づいて優先権を主張するとともに、優先権を主張する本出願の出願日よりも前の出願日を有する外国での特許出願または発明者証の出願、或いはPCT国際出願については、いかなる出願も、下記の枠内をチェックすることにより示した。

I hereby claim foreign priority foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filling date before that of the application for which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願日／月／年)	
Hei 11-304700	Japan	26 October 1999	☐
Hei 11-304701	Japan	26 October 1999	☐

私は、ここに、下記のいかなる米国仮特許出願についても、その米国法典第35編119条(e)項の利益を主張する。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、ここに、下記のいかなる米国出願についても、その米国法典第35編120条に基づく利益を主張し、又米国を指定するいかなるPCT国際出願についても、その同第365条(c)に基づく利益を主張する。また、本出願の各特許請求の範囲の主題が、米国法典第35編第112条第1段に規定された態様で、先行する米国出願又はPCT国際出願に開示されていない場合においては、その先行出願の出願日と本国内出願日またはPCT国際出願日との間の期間中に入手された情報で、連邦規則法典37編規則1.56に定義された特許性に関わる重要な情報について開示義務があることを承認する。

Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filling date of the prior application and the national or PCT International filing date of application.

I hereby claim the benefit under Title 35, United States

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現状：特許許可、係属中、放棄)

Japanese language Declaration
(日本語宣言書)

私は、ここに表明された私自身の知識に係わる陳述が真実であり、且つ情報と信ずることに基づく陳述が、事実であると信じられることを宣言し、さらに、故意に虚偽の陳述などを行った場合は、米国法典第 18 編第 1001 条に基づき、罰金または拘禁、若しくはその両方により処罰され、またそのような故意による虚偽の陳述は、本出願またはそれに対して発行されるいかなる特許も、その有効性に問題が生ずることを理解した上で陳述が行われたことを、ここに宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

委任状： 私は本出願を審査する手続きを行い、且つ米国特許商標庁との全ての業務を遂行するために、記名された発明者として、下記の弁護士及び／または弁理士を任命する。(氏名及び登録番号を記載すること)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

Anthony B. Askew - 24,154; Roger T. Frost - 22,176; Robert E. Richards - 29,105; Stephen M. Schaetzel -31,418; Larry A. Roberts - 31,871; Peter G. Pappas - 33,205; James Dean Johnson - 31,771; Daniel J. Warren - 34,272; Leona G. Young - 37,266; Jamie L. Greene-32,467; Mary Anthony Merchant - 39,771; William L. Warren - 36,714; Brenda Ozaki Holmes - 40,339; James D. Withers - 40,376; Kimberly J. Prior - 41,483; Theodore M. Green - 41,801; John K. McDonald - 42,860; Michael S. Pavento - 42,985; Suzanne Seavello Shope - 37,933; Sima Singadia Kulkarni - 43,732; Christopher J. Chan - 44,070; John M. Briski - 44,562; Lisa C. Elsevier - 44,669; S. Craig Hemenway - 44,759; Paul E. Knowlton - 44,842; Charles E. Peeler - 45,004; Cheryl L. Huseman - 45,392; Adam Avrunin - 45,457; Shelby B. Grier - 45,785; Vaibhav P. Kadaba - 45,865; Donald R. Andersen - 28,280.

書類送付先 Send Correspondence to:

KILPATRICK STOCKTON LLP 2400 Monarch Tower, 3424 Peachtree Road, N.E., Atlanta, GA 30326

直通電話連絡先：(氏名及び電話番号) Direct Telephone calls to: (name and telephone number)

Roger T. Frost at (404) 949-2400

唯一または第一発明者氏名		Full name of sole or first inventor Satoshi KITAGAWA
発明者の署名	日付	Inventor's signature Date Satoshi Kitagawa 26 October 1999
住所		Residence Kanagawa, Japan
国籍		Citizenship Japan
郵便の宛先		Post Office Address c/o KOMATSU DENSHI KINZOKU KABUSHIKI KAISHA 2612, Shinomiya Hiratsuka-shi, Kanagawa 254-0014 Japan
第二共同発明者がいる場合、その氏名		Full name of second joint inventor, if any
第二共同発明者の署名	日付	Second inventor's signature Date
住所		Residence
国籍		Citizenship
郵便の宛先		Post Office Address

(第三以下の共同発明者についても同様に記載し、署名をすること) (Supply similar information and signature for third and subsequent joint inventors.)